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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al. Art Unit: 2666
Serial No.: 10/024,657 Examiner: Jay P. Patel
Filed : December 18, 2001
Assignee : Intel Corporation
Title : CONTROL MECHANISMS FOR ENQUEUE AND DEQUEUE
OPERATIONS IN A PIPELINED NETWORK PROCESSOR

Mail Stop Amendment

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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Applicants call attention to the attached Information
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Kindly accept this Information Disclosure Statement under
Rule 97(c)(2). The rule 17(p) certification fee of \$180 is
enclosed.

The documents are in the English language; hence no concise
explanation is necessary per Rule 98(a)(3).

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Applicant : Gilbert Wolrich et al.
Serial No. : 10/024,657
Filed : December 18, 2001
Page : 2 of 2

Attorney's Docket No.: 10559-613001 / P12852

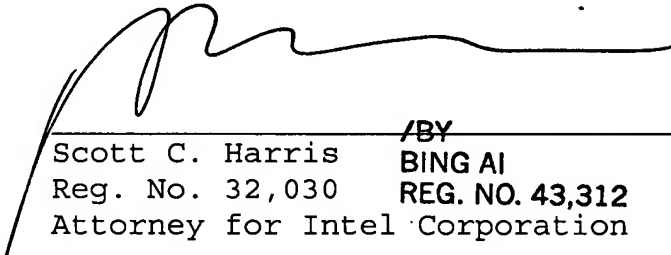


Consideration of the foregoing and enclosures plus the
return of a copy of the enclosed form PTO-1449 with the
Examiner's initials in the left column per MPEP 609 are
earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit
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Respectfully submitted,

Date: January 17, 2006



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U.S. Department of Commerce
Patent and Trademark Office

Attorney's Docket No.

10559-613001

Application No.

10/024,657

**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

Applicant

Gilbert Wolrich et al.

Filing Date

December 18, 2001

Group Art Unit

2666

(37 CFR §1.98(b))

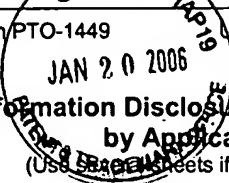
U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2001/0014100	08/2001	Abe et al.			
	AB	2002/0131443	09/2002	Robinett et al.			
	AC	2002/0144006	10/2002	Cranston et al.			
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	AG	2003/0115347	06/2003	Wolrich et al.			
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	AAA	6,684,303	01/2004	LaBerge			

Examiner Signature

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EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Form PTO-1449 (Modified)  Information Disclosure Statement by Applicant (Use separate sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-613001	Application No. 10/024,657
	Applicant Gilbert Wolrich et al.		
	Filing Date December 18, 2001	Group Art Unit 2666	

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	6,724,721	04/2004	Cheriton			
	ACC	6,757,791	06/2004	O'Grady et al.			
	ADD	6,768,717	07/2004	Reynolds et al.			
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	AHH	6,822,958	11/2004	Branth et al.			
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	AJJ						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AKK	0 418 447	03/1991	Europe				
	ALL	0 760 501	03/1997	Europe				
	AMM	WO 98/25210	06/1998	WIPO				
	ANN	WO 03/017541	02/2003	WIPO				
	AOO							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	APP	Adiletta, et al., "The next generation of Intel IXP Network Processors", Intel Technology Journal, Network Processors, vol. 6, issue 3, published Aug. 15, 2002, pp. 6-18.
	AQQ	Brewer, et al., "Remote Queues: Exposing Message Queues for Optimization and Atomicity", SPAA '95 Santa Barbara, CA, pp. 1-13.
	ARR	Buyuktosunoglu, A., et al., "Tradeoffs in Power-Efficient Issue Queue Design", ISLPED '02, ACM, Aug. 2002, 6 pages.
	ASS	Dandamudi, S., "Multiprocessors", IEEE Computer, Mar. 1997, pp. 82-89.
	ATT	Hendler, D., et al., "Work Dealing", SPAA '02, ACM, Aug. 2002, pp. 164-172.
	AUU	Jonkers, H., "Queueing Models of Shared-Memory Parallel Applications", Computer and Telecommunications Systems Performance Engineering, Pentech Press, London, 1994, 13 pages.

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Substitute Form PTO-1449
(Modified)U.S. Department of Commerce
Patent and Trademark OfficeAttorney's Docket No.
10559-613001Application No.
10/024,657**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

(37 CFR § 1.538(b))

Applicant
Gilbert Wolrich et al.Filing Date
December 18, 2001Group Art Unit
2666**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AVV	Kornaros, et al., "A Fully-Programmable Memory Management System Optimizing Queue Handling at Multi Gigabit Rates", ACM, Jun. 2-6, 2003, pp. 54-59.
	AWW	Kumar, S., et al., "A Scalable, Cache-Based Queue Management Subsystem for Network Processors", no date, pp. 1-7.
	AXX	Lymar, T., et al., "Data Streams Organization in Query Executor for Parallel DBMS", no date, 4 pages.
	AYY	McLuckie, L., et al., "Using the RapidIO Messaging Unit on PowerQUICC III", Freescale Semiconductor, Inc., 2004 Rev. 1, pp. 1-19.
	AZZ	Michael, M., "Scalable Lock-Free Dynamic Memory Allocation", PLDI '04, ACM, Jun. 2004, pp. 1-12.
	AAAA	Pan, H., et al., "Heads and Tails: A Variable-Length Instruction Format Supporting Parallel Fetch and Decode", CASES 01, No. 16-17, 2001, 8 pages.
	ABBB	Scott, M., "Non-Blocking Timeout in Scalable Queue-Based Spin Locks", PODC '02, ACM, Jul. 2002, pp.31-40.
	ACCC	

Examiner Signature

Date Considered

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